EENG 5550 HW 1

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# Block diagram of ALU

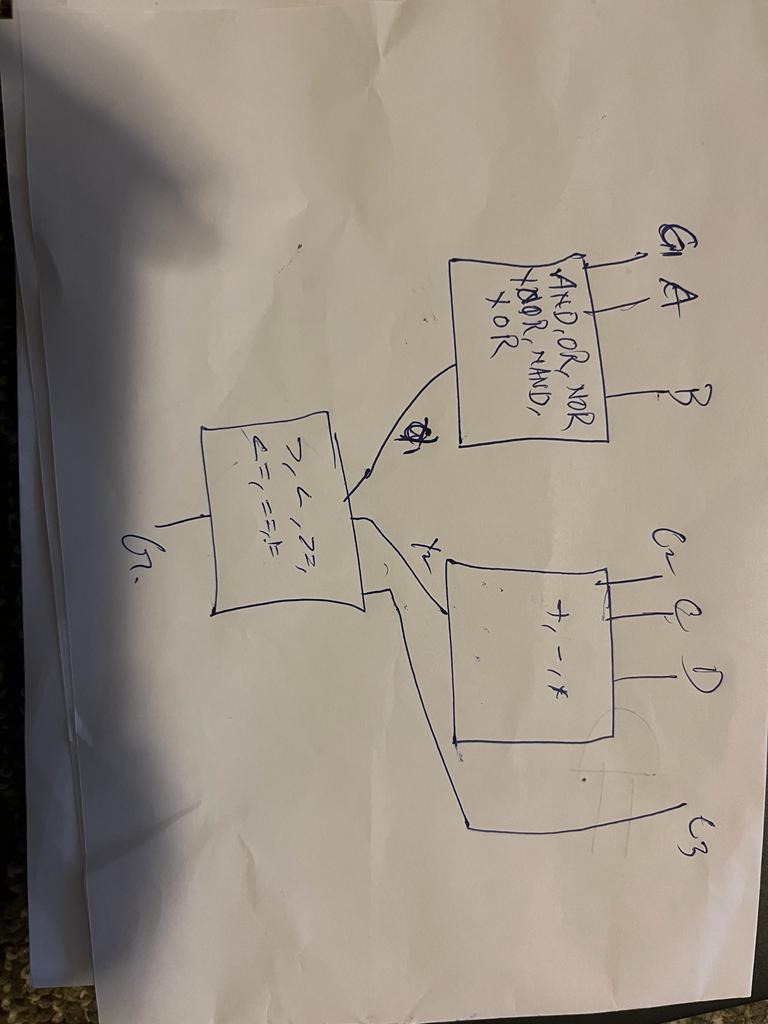


Figure 1 ALU

* Overall Component: alu
* Overall ports:
  + Inputs: A, B, C, D
    - C1, C2, C3
  + Outputs:
    - G
* Necessary intermediate signals:
  + Y1
  + Y2

## Design\Algorithm ex:

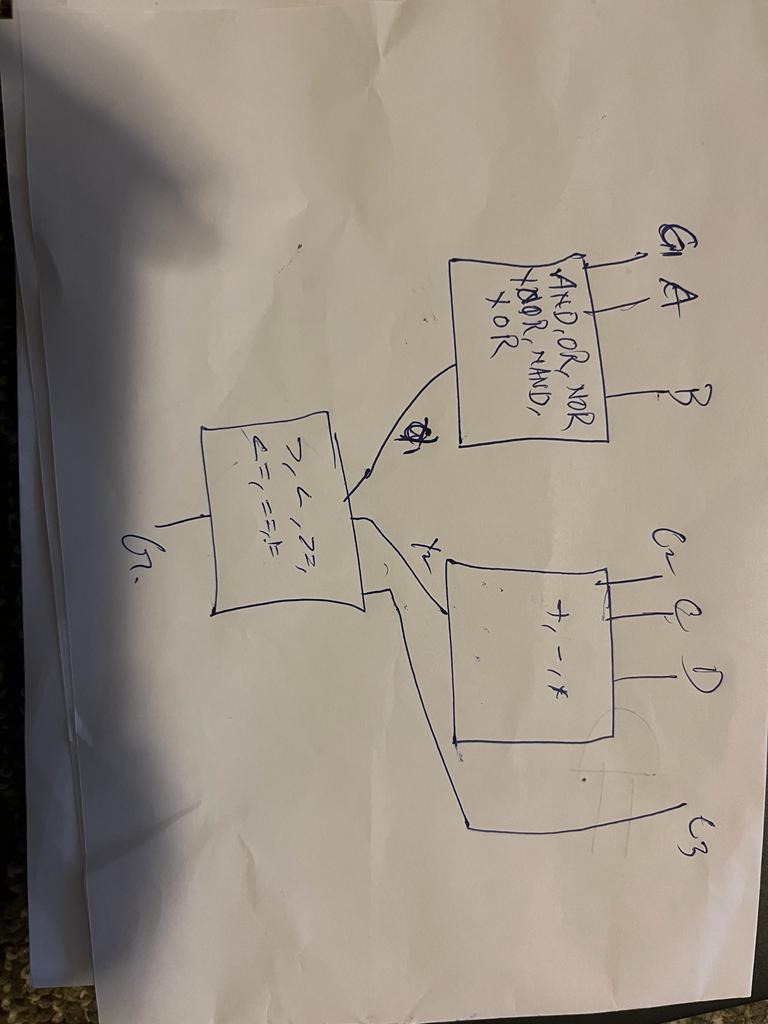


Figure 2– ALU

* Overall Component: ALU
* Overall ports:
  + Inputs:
    - A
    - B
    - C
    - D
    - C1
    - C2
    - C3
  + Outputs:
    - G

# Generated RTL Block Diagram\Schematic

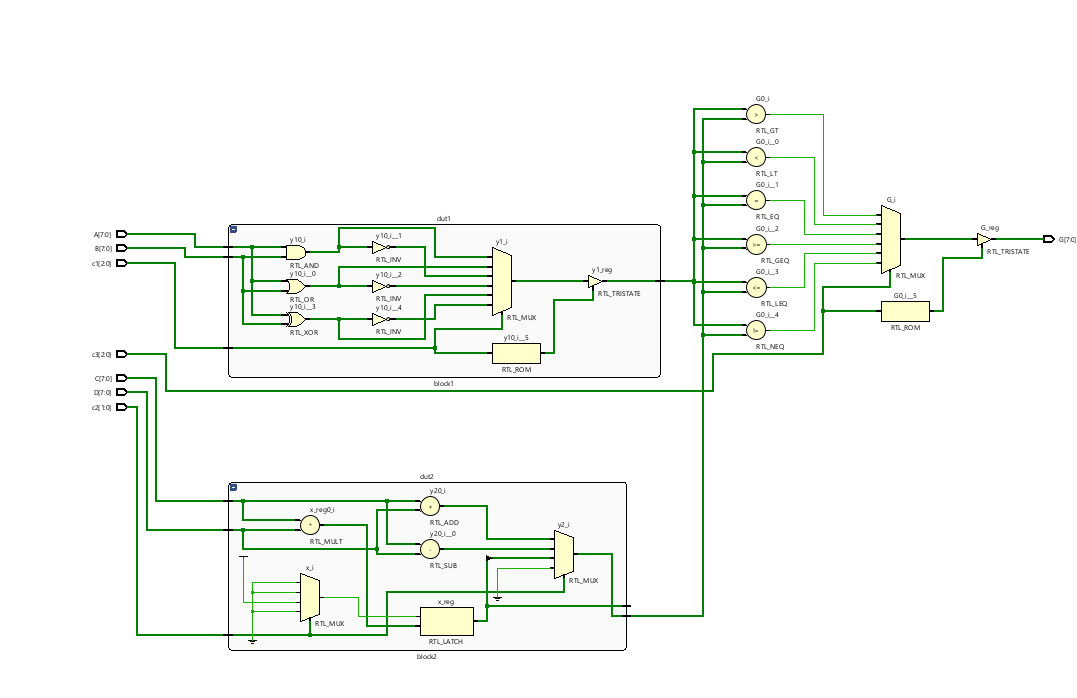


Figure 5 - ALU

# Results

## Waveforms

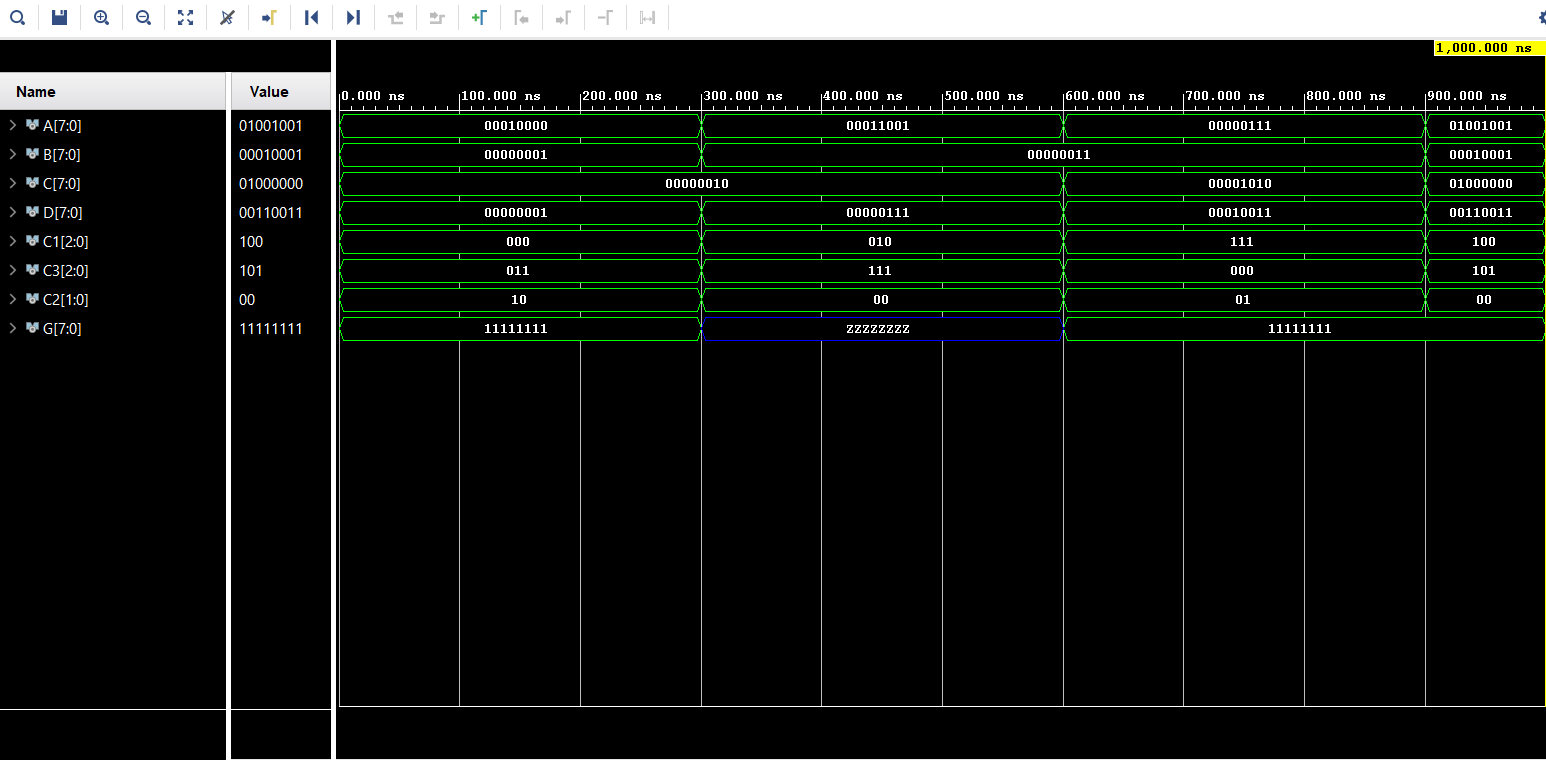


Figure 6 - Waveforms

## Table

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  | calculations | waveforms |  |
|  | A | B | C | D | C1 | C2 | C3 | Y | Y | |
| Test case 1: | 00010000 | 00000001 | 00000010 | 00000001 | 000 | 10 | 011 | 11111111 | 11111111 | |
| Test case 2: | 00000111 | 00000011 | 00001010 | 00010011 | 111 | 01 | 000 | 00010 | ZZZZZZZZ | |